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## EE/EX-4003-CBGS

### B.E. IV Semester

Examination, December 2020

### Choice Based Grading System (CBGS)

### Digital Electronics Logic Design

Time : Three Hours

Maximum Marks : 70

- Note:** i) Attempt any five questions.  
ii) All questions carry equal marks.

1. a) Convert the following:
  - i)  $(0.828125)_{10} = (?)_2$
  - ii)  $(18.6)_9 = (?)_{11}$
  - iii)  $(234)_{10} = (?)_8$
  - iv)  $(AF.16C)_{16} = (?)_8$
  - v)  $(4163)_{10} + (7520)_8 = (?)_2$
- b) Explain error detecting and correcting codes with examples.
2. a) Implement  $f(x, y, z) = \sum m(0, 3, 4, 5, 7)$  in NAND logic.  
b) Design a 32101 multiplexer using 8 to 1 multiplexers having an active LOW ENABLE input and a 2-to-4 decoder.
3. a) What do you understand by Universal Gate. Design AND, OR and NOT gates using NOR gate only.  
b) What do you understand by Multiplexer? Implement the following function using 8\*1 multiplexer  
 $F(A, B, C, D) = \sum(0, 1, 3, 4, 8, 9, 15)$

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4. a) What is Latch? What are the difference between Latch and Flip Flop? Explain D latch with truth table and logic diagram.  
b) Explain J and K Flip Flop with truth table and logic diagram.
5. a) Define the following and explain:
  - i) State Diagram
  - ii) State Table
  - iii) State Equation
  - iv) State Assignmentb) Explain the working of Johnson counter with suitable diagram.
6. a) What do you understand by Counter? Give the difference between Synchronous and Asynchronous counter.  
b) What is Shift Register? What are different types of shift registers? Explain.
7. a) Explain the working of BCD counter.  
b) Discuss the principle working of programmable array logic.
8. Write short notes on :
  - a) Encoder and Decoder
  - b) PLD

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